What Is Claimed Is:

1. A data recovery circuit, comprising:

a clock generator for generating a first group of sampling clock pulses and a second group of sampling clock pulses for sampling an incoming data stream, each sampling edge of said first group of sampling clock pulses and each sampling edge of said second group of sampling clock pulses being arranged alternatively and being separated from each other for an interval equal to half the period of said incoming data stream, said clock generator being controlled in response to a phase control signal to adjust phases of said first group of sampling clock pulses and said second group of sampling clock pulses;

a data and phase sampling circuit for receiving said incoming data stream, said first group of sampling clock pulses and said second group of sampling clock pulses, said data and phase sampling circuit taking samples of said incoming data stream in accordance with said first group of sampling clock pulses to produce a first sampled data stream while taking samples of said incoming data stream in accordance with said second group of sampling clock pulses to produce a second sampled data stream; and

a phase detection and correction circuit coupled to said data and phase sampling circuit, for determining resemblances of each bit in said second sampled data stream to the corresponding two bits in said first sampled data stream, the associated sampling edge of said bit in said second sampled data stream being adjacent to the associated sampling edges of said two bits in said first sampled data stream, said phase detection and

correction circuit producing said phase control signal on the basis of the resemblance determination result.

2. The data recovery circuit of claim 1, wherein said first sampled data stream is used as a data recovery output.

3. The data recovery circuit of claim 1, wherein said first group of sampling clock pulses and said second group of sampling clock pulses have the same frequency, which is equal to half the frequency of said incoming data stream.

4. The data recovery circuit of claim 3, wherein said first group of sampling clock pulses includes a first clock signal and said second group of sampling clock pulses includes a second clock signal, said first clock signal and said second clock signal being 90 degrees out of phase with each other, and both rising edges and falling edges of said first clock signal and said second clock signal being used as said sampling edges.

5. The data recovery circuit of claim 3, wherein said first group of sampling clock pulses includes a first clock signal and a third clock signal and said second group of sampling clock includes a second clock signal and a forth clock signal, said first clock signal and said second clock signal being 90 degrees out of phase with each other, said first clock signal and said third clock signal being 180 degrees out of phase with each other, and said second clock signal and said forth clock signal being 180 degrees out of phase with each other.

6. The data recovery circuit of claim 5, wherein rising edges of said first to said forth clock signals are used as said sampling edges.

7. The data recovery circuit of claim 5, wherein falling edges of said first to said forth clock signals are used as said sampling edges.

8. The data recovery circuit of claim 1, wherein said first group of sampling clock pulses and said second group of sampling clock pulses have the same frequency, which is equal to the frequency of said incoming data stream.

9. The data recovery circuit of claim 1, further comprising a demultiplexer coupled between said data and phase sampling circuit and said phase detection and correction circuit, for converting said first sampled data stream and said second sampled data stream from serial data to parallel data.

10. The data recovery circuit of claim 1, wherein said phase detection and correction circuit comprises:

an early/late determination circuit for receiving said first sampled data stream and said second sampled data stream and determining resemblances of each bit in said second sampled data stream to the corresponding two bits in said first sampled data stream, the associated sampling edge of said bit in said second sampled data stream being adjacent to the associated sampling edges of said two bits in said first sampled data stream, said early/late determination circuit selectively producing an early signal and a late signal;

an early/late summation circuit for receiving said early signal and said late signal and producing an early/late summation signal on the basis of a summation result of said early signal and said late signal; and

a low pass filter for receiving said early/late summation signal and producing said phase control signal.

11. The data recovery circuit of claim 10, wherein said early/late determination circuit comprises:

a resemblance detection circuit for detecting whether or not said corresponding two bits in said first sampled data stream are the same, detecting whether said bit in said second sampled data stream is equal to the former or the latter of said corresponding two bits if said two bits are not the same, and accordingly producing a resemblance signal of said bit; and

an early/late decision circuit for receiving the resemblance signals of a predetermined number of bits, comparing the number of times that said bit is equal to the former of said corresponding two bits with the number of times that said bit is equal to the latter of said corresponding two bits, and selectively producing said early signal or said late signal.

12. The data recovery circuit of claim 10, wherein said early/late summation circuit performs an addition operation to add one to an accumulative amount responsive to receiving said early signal while performs an subtraction operation to subtract one from the accumulative amount responsive to receiving said late signal and outputs the accumulative amount as said early/late summation signal, and wherein said low pass filter produces said phase control signal on the basis of the polarity of said early/late summation signal obtained after a predetermined times of summation operations by said early/late summation circuit.

13. A phase detection circuit for detecting phase conditions of a first group of sampling clock pulses and a second group of sampling clock pulses in a data recovery circuit, said first group of sampling clock pulses being used for sampling approximately a central portion of each data bit in an incoming data stream to produce a first sampled data stream while said second group of sampling clock pulses being used for sampling approximately a transition portion between every two data bits in said incoming data stream to produce a second sampled data stream, said phase detection circuit comprising:

an early/late determination circuit for receiving said first sampled data stream and said second sampled data stream, comprising:

a resemblance detection circuit including a plurality of resemblance detecting units, each of said plurality of resemblance detecting units being used for detecting whether one of a plurality of bits in said second sampled data stream is equal to the former or the latter of the corresponding two bits in said first sampled data stream and producing one of a plurality of resemblance signals; and

an early/late decision circuit for receiving said plurality of resemblance signals corresponding to said plurality of bits, comparing the number of times that one bit is equal to the former of the corresponding two bits with the number of times that one bit is equal to the latter of the corresponding two bits, and selectively producing an early signal or a late signal.

14. The phase detection circuit of claim 13, further comprising an early/late summation circuit for receiving

said early signal and said late signal and producing an early/late summation signal on the basis of a summation result of said early signal and said late signal.

15. The phase detection circuit of claim 14, wherein said early/late summation circuit performs an addition operation to add one to an accumulative amount responsive to receiving said early signal while performs an subtraction operation to subtract one from the accumulative amount responsive to receiving said late signal and outputs the accumulative amount as said early/late summation signal.

16. A phase detection circuit for detecting phase conditions of a first group of sampling clock pulses and a second group of sampling clock pulses in a data recovery circuit, said first group of sampling clock pulses being used for sampling approximately a central portion of each data bit in an incoming data stream to produce a first sampled data stream while said second group of sampling clock pulses being used for sampling approximately a transition portion between every two data bits in said incoming data stream to produce a second sampled data stream, said phase detection circuit comprising:

an early/late determination circuit for receiving said first sampled data stream and said second sampled data stream, said early/late determination circuit determining a resemblance of said first sampled data stream and said second sampled data stream by detecting whether one bit in said second sampled data stream is equal to the former or the latter of the corresponding two bits in said first sampled data stream and producing an early signal or a late signal; and

an early/late summation circuit for receiving said early signal and said late signal and producing an early/late summation signal on the basis of a summation result of said early signal and said late signal.

17. A data recovery circuit, comprising:

a clock generator for generating a first group of sampling clock pulses and a second group of sampling clock pulses for sampling an incoming data stream, each sampling edge of said first group of sampling clock pulses and each sampling edge of said second group of sampling clock pulses being arranged alternatively and being separated from each other for an interval equal to half the period of said incoming data stream, said clock generator being controlled in response to a phase control signal to adjust phases of said first group of sampling clock pulses and said second group of sampling clock pulses;

a data and phase sampling circuit for receiving said incoming data stream, said first group of sampling clock pulses and said second group of sampling clock pulses, said data and phase sampling circuit taking samples of approximately a central portion of each data bit in said incoming data stream in accordance with said first group of sampling clock pulses to produce a first sampled data stream while taking samples of approximately a transition portion of every two bits in said incoming data stream in accordance with said second group of sampling clock pulses to produce a second sampled data stream; and

a phase detection and correction circuit coupled to said data and phase sampling circuit, for determine

resemblances of each bit in said second sampled data stream to the corresponding two bits in said first sampled data stream, said phase detection and correction circuit defining an early condition for the phases of said first group of sampling clock pulses and said second group of sampling clock pulses if each bit in said second sampled data stream resembles the former of the corresponding two bits in said first sampled data stream while defining a late condition for the phases of said first group of sampling clock pulses and said second group of sampling clock pulses if each bit in said second sampled data stream resembles the latter of the corresponding two bits in said first sampled data stream, and producing said phase control signal on the basis of said early condition or said late condition to adjust the phases of said first group of sampling clock pulses and said second group of sampling clock pulses by shifting the phases backwards or forwards.

18. The data recovery circuit of claim 17, wherein said first sampled data stream is used as a data recovery output.

19. The data recovery circuit of claim 17, wherein said first group of sampling clock pulses and said second group of sampling clock pulses have the same frequency, which is equal to half the frequency of said incoming data stream.

20. The data recovery circuit of claim 19, wherein said first group of sampling clock pulses includes a first clock signal and said second group of sampling clock pulses includes a second clock signal, said first clock signal and said second clock signal being 90 degrees out of phase with each other, and both rising edges and falling edges

of said first clock signal and said second clock signal being used as said sampling edges.

21. The data recovery circuit of claim 19, wherein said first group of sampling clock pulses includes a first clock signal and a third clock signal and said second group of sampling clock includes a second clock signal and a forth clock signal, said first clock signal and said second clock signal being 90 degrees out of phase with each other, said first clock signal and said third clock signal being 180 degrees out of phase with each other, and said second clock signal and said forth clock signal being 180 degrees out of phase with each other.

22. The data recovery circuit of claim 21, wherein rising edges of said first to said forth clock signals are used as said sampling edges.

23. The data recovery circuit of claim 21, wherein falling edges of said first to said forth clock signals are used as said sampling edges.

24. The data recovery circuit of claim 17, wherein said first group of sampling clock pulses and said second group of sampling clock pulses have the same frequency, which is equal to the frequency of said incoming data stream.

25. The data recovery circuit of claim 17, further comprising a demultiplexer coupled between said data and phase sampling circuit and said phase detection and correction circuit, for converting said first sampled data stream and said second sampled data stream from serial data to parallel data.

26. The data recovery circuit of claim 17, wherein said phase detection and correction circuit comprises:

an early/late determination circuit for receiving said first sampled data stream and said second sampled data stream, determining whether each bit in said second sampled data stream resembles the former or the latter of the corresponding two bits in said first sampled data stream, and selectively producing an early signal or a late signal;

an early/late summation circuit for receiving said early signal and said late signal and producing an early/late summation signal on the basis of a summation result of said early signal and said late signal; and

a low pass filter for receiving said early/late summation signal and producing said phase control signal to adjust the phases of said first group of sampling clock pulses and said second group of sampling clock pulses by shifting the phases backwards or forwards.

27. The data recovery circuit of claim 26, wherein said early/late summation circuit performs an addition operation to add one to an accumulative amount responsive to receiving said early signal while performs an subtraction operation to subtract one from the accumulative amount responsive to receiving said late signal and outputs the accumulative amount as said early/late summation signal, and wherein said low pass filter produces said phase control signal on the basis of the polarity of said early/late summation signal obtained after a predetermined times of summation operations by said early/late summation circuit.

28. A method for detecting and correcting phase conditions

in a data recovery circuit, comprising:

sampling approximately a central portion of each data bit in an incoming data stream in accordance with a first group of sampling clock pulses to produce a first sampled data stream while sampling approximately a transition portion between every two data bits in said incoming data stream in accordance with a second group of sampling clock pulses to produce a second sampled data stream;

detecting whether each bit in said second sampled data stream resembles the former or the latter of the corresponding two bits in said first sampled data stream;

summarizing a plurality of detection results produced in said detecting step to determine whether the phases of said first group of sampling clock pulses and said second group of sampling clock pulses are in an early condition or in a late condition; and

adjusting the phases of said first group of sampling clock pulses and said second group of sampling clock pulses by shifting the phases backwards or forwards on the basis of said early condition or said late condition.

29. A method for detecting and correcting phase conditions in a data recovery circuit, comprising:

sampling approximately a central portion of each data bit in an incoming data stream in accordance with a first group of sampling clock pulses to produce a first sampled data stream while sampling approximately a transition portion between every two data bits in said incoming data stream in accordance with a second group of sampling clock pulses to produce a second sampled data stream;

combining a predetermined number of bits in said first sampled data stream into a group to form a plurality of

first sampled data groups and combining a predetermined number of bits in said second sampled data stream into a group to form a plurality of second sampled data groups;

for each first sampled data group and the corresponding second sampled data group, detecting whether each bit in said second sampled data stream is equal to the former or the latter of the corresponding two bits in the first sampled data stream and respectively counting the number of times that said bit is equal to the former of said corresponding two bits and the number of times that said bit is equal to the latter of said corresponding two bits;

for each first sampled data group and the corresponding second sampled data group, producing an early signal if the number of times that said bit is equal to the former of said corresponding two bits is greater than the number of times that said bit is equal to the latter of said corresponding two bits, and producing a late signal if the number of times that said bit is equal to the latter of said corresponding two bits is greater than the number of times that said bit is equal to the former of said corresponding two bits;

summarizing a plurality of early signals and late signals to determine whether the phases of said first group of sampling clock pulses and said second group of sampling clock pulses are in a early condition or in a late condition; and

adjusting the phases of said first group of sampling clock pulses and said second group of sampling clock pulses by shifting the phases backwards or forwards on the basis of said early condition or said late condition.

30. The method of claim 29, wherein said step of summarizing

a plurality of early signals and late signals is carried out by performing an addition operation to add one to an accumulative amount responsive to receiving said early signal while performing an subtraction operation to subtract one from the accumulative amount responsive to receiving said late signal and outputting the accumulative amount as an early/late summation signal.

31. The method of claim 30, wherein said step of adjusting the phases of said first group of sampling clock pulses and said second group of sampling clock pulses by shifting the phases backwards or forwards is performed on the basis of the polarity of said early/late summation signal.